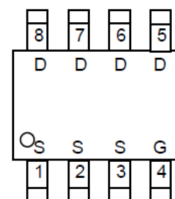
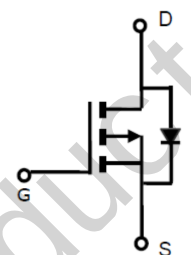


FEATURE

- ◆ -30V/-5.8A, $R_{DS(ON)}=38m\Omega$ (typ.)@ $V_{GS}=-10V$
- ◆ -30V/-4.0A, $R_{DS(ON)}=60m\Omega$ (typ.)@ $V_{GS}=-4.5V$
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ SOP8 package design



TOP VIEW
SOP-8



P-Channel

DESCRIPTION

The APM9435 is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching

APPLICATIONS

- ◆ High Frequency Point-of-Load Synchronous
- ◆ Newworking DC-DC Power System
- ◆ Load Switch

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V _{DSS}	Drain-Source Voltage		-30	V
V _{GSS}	Gate-Source Voltage		±20	V
I _D	Continuous Drain Current (T _A =25°C)	V _{GS} =10V	-5.8	A
	Continuous Drain Current (T _A =75°C)		-4.2	A
I _{DM}	Pulsed Drain Current		-20	A
I _S	Continuous Source Current (Diode Conduction)		-2.0	A
P _D	Power Dissipation	T _A =25°C	2.05	W
		T _A =70°C	1.5	
T _J	Operation Junction Temperature		150	°C
T _{STG}	Storage Temperature Range		-55~+150	°C
R _{θJA}	Thermal Resistance Junction to Ambient		85	°C/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress rating only and functional device operation is not implied

■ **ELECTRICAL CHARACTERISTICS** ($T_A=25^\circ\text{C}$ Unless otherwise noted)

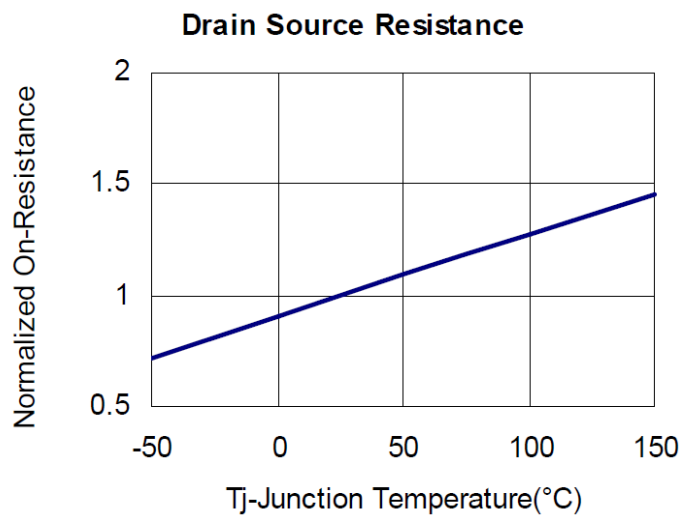
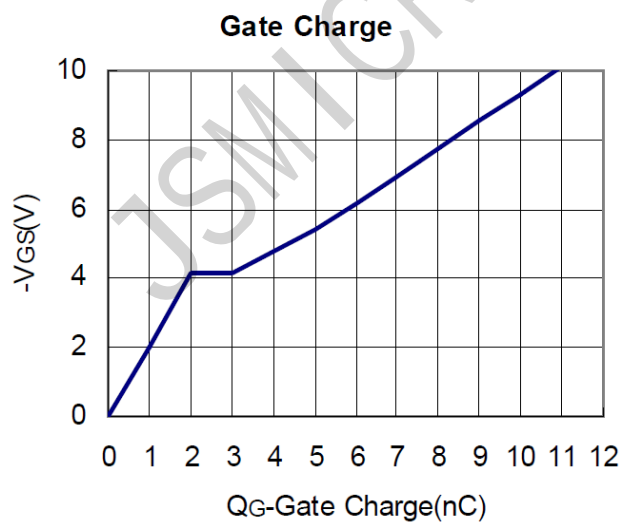
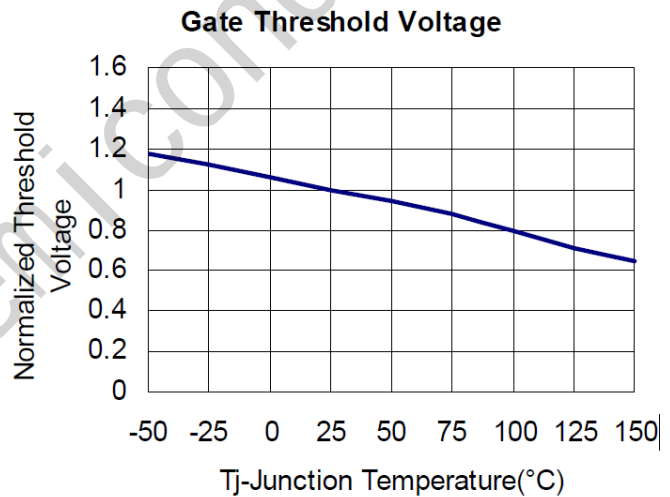
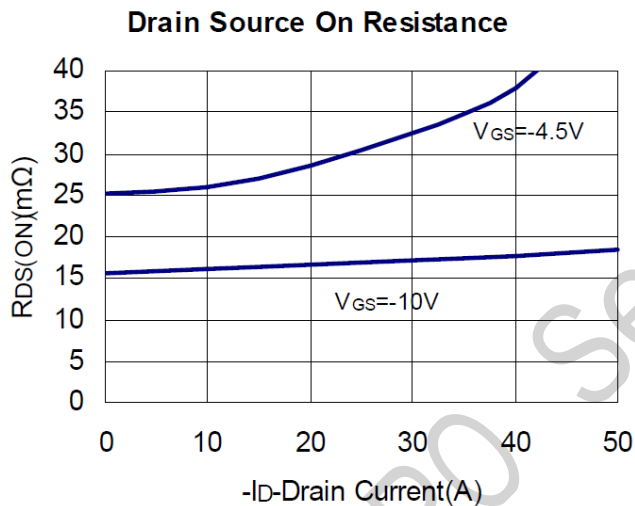
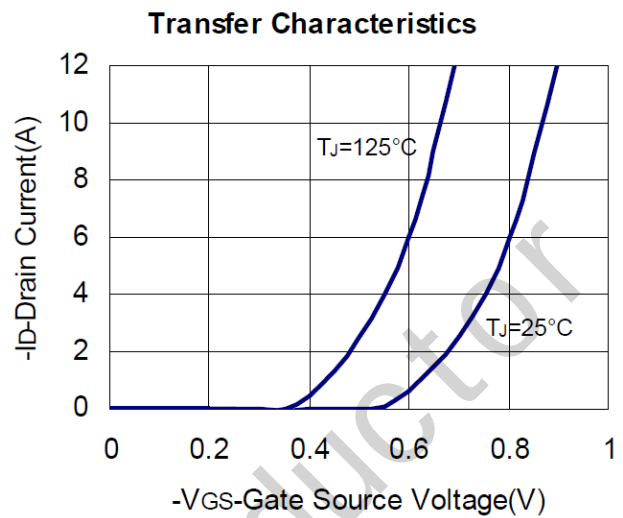
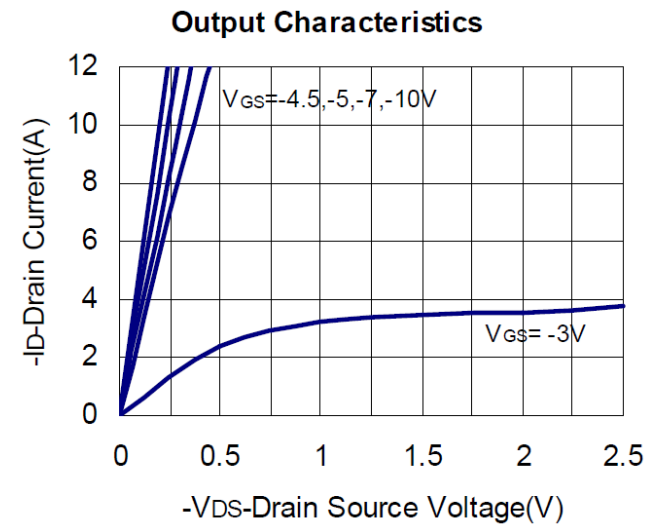
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1.0		-2.5	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0			-1	uA
		V _{DS} =-24V, V _{GS} =0 T _J =55℃			-5	
R _{DS(ON)}	Drain-Source On-Resistance	V _{GS} =-10V, I _D =-10A		38	48	mΩ
		V _{GS} =-4.5V, I _D =-6.0A		60	78	
Source-Drain Diode						
V _{SD}	Diode Forward Voltage	I _S =-2.0A, V _{GS} =0V		-0.7	-1.2	V
Dynamic Parameters						
Q _g	Total Gate Charge	V _{DS} =-20V V _{GS} =-10V I _D =-5.8A		6.2		nC
Q _{gs}	Gate-Source Charge			2.5		
Q _{gd}	Gate-Drain Charge			3.3		
C _{iss}	Input Capacitance	V _{DS} =-15V V _{GS} =0V f=1MHz		640		pF
C _{oss}	Output Capacitance			270		
C _{rss}	Reverse Transfer Capacitance			103		
T _{d(on)}	Turn-On Time	V _{DS} =-15V I _D =-5A		9.2		nS
T _r				16.5		
T _{d(off)}	Turn-Off Time	V _{GEN} =-10V R _G =3.3Ω		21.3		
T _f				21.5		

Note: 1. Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

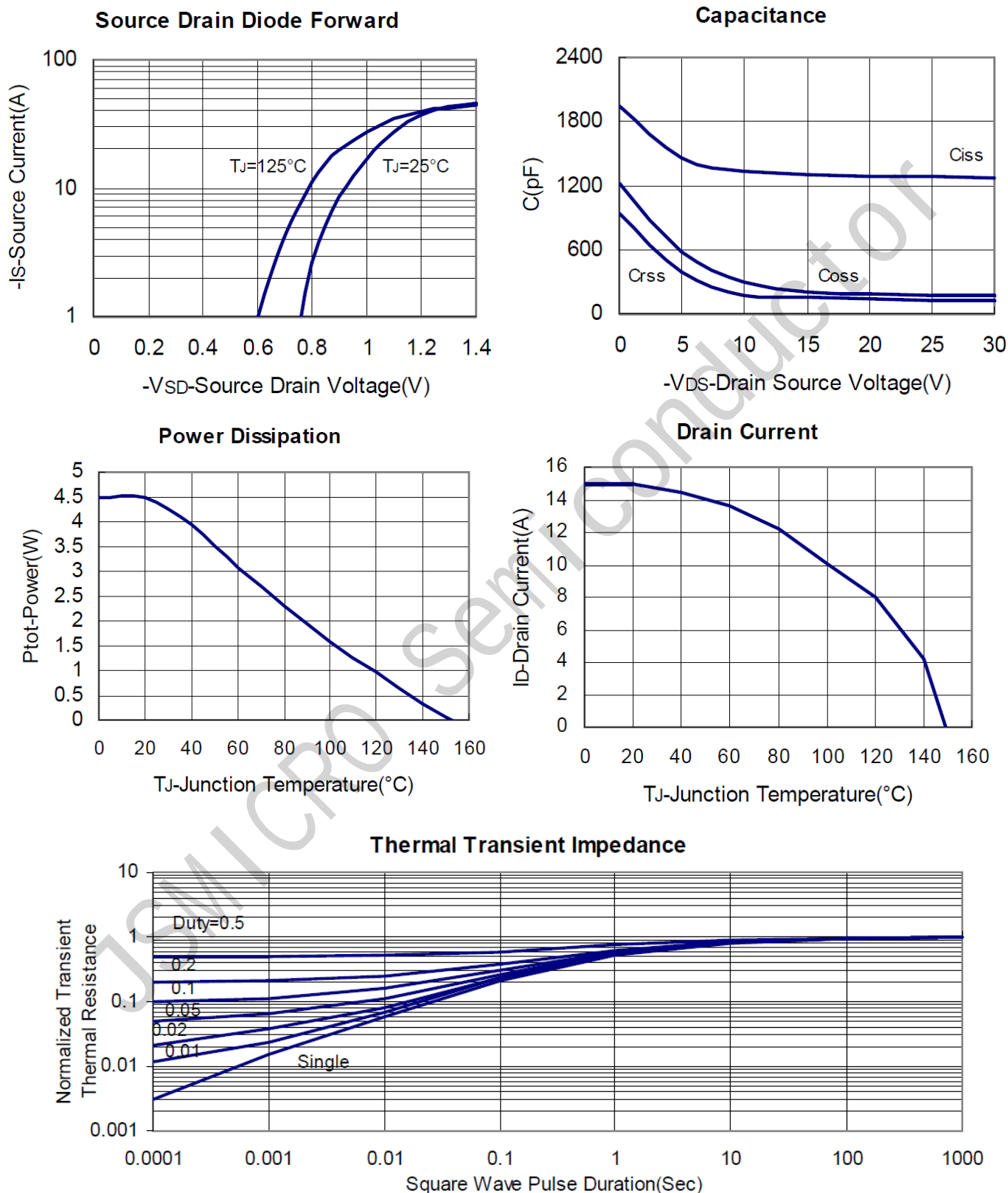
2. Static parameters are based on package level with recommended wire bonding



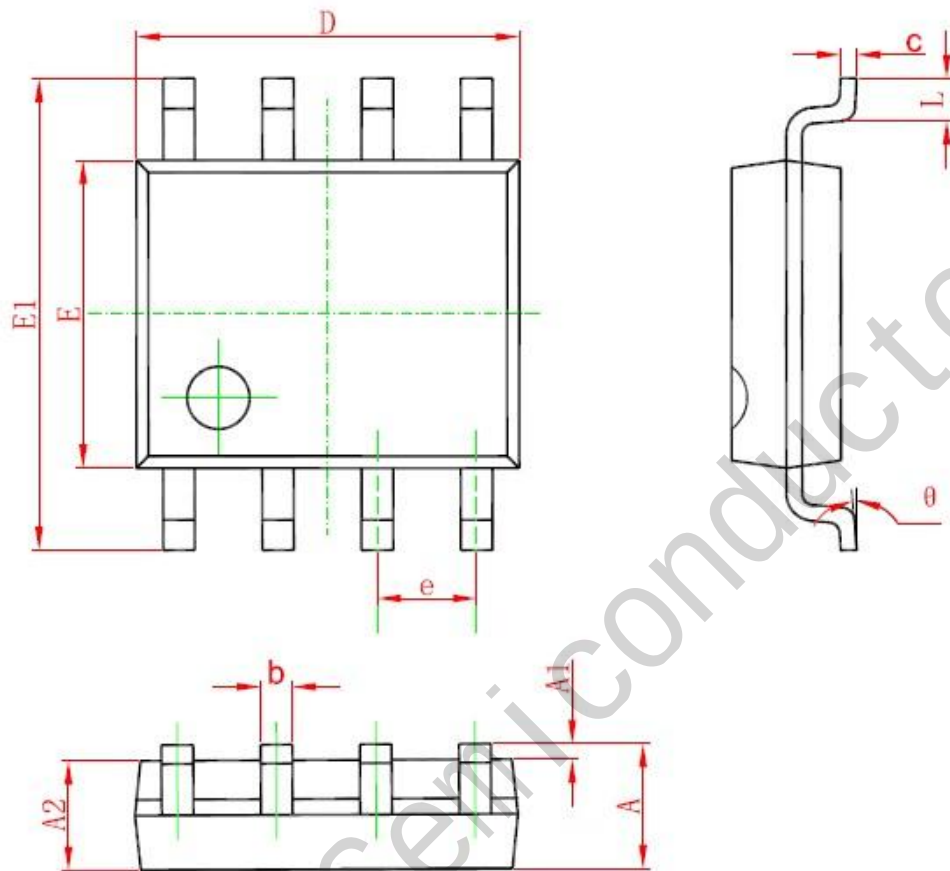
■ **TYPICAL CHARACTERISTICS** (25°C Unless Note)



■ TYPICAL CHARACTERISTICS (continuous)



■ SOP8 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°